SYSTEM OVERVIEW & INTERFACE SPECIFICATION

VEB Keramische Werke Hermsdorf Ferritkerne VEB 5221.3 (0.8mm) • Halbauswahlstrom Im/2 = 350 mA, Vollstrom Im = 700 mA • 45° diagonale Sense-Leseschleife für induktive mV-Spannungsspitzen (Delta V ~ 30mV) • Horizontale/Vertikale Koinzidenz-Fädelmatrix.

X-AXIS HALF-SELECT DRIVERS (X0 .. X31)

32 Koinzidenz-Halbstromleitungen (350 mA Puls, Tr < 50 ns).

- ◇X_IN_0
- ◇X_IN_1
- ◇X_IN_2
- ◇X_IN_3
- ◇X_IN_4
- ◇X_IN_5
- ◇X_IN_6
- ◇X_IN_7
- ◇X_IN_8
- ◇X_IN_9
- ◇X_IN_10
- ◇X_IN_11
- ◇X_IN_12
- ◇X_IN_13
- ◇X_IN_14
- ◇X_IN_15
- ◇X_OUT_0
- ◇X_OUT_1
- ◇X_OUT_2
- ◇X_OUT_3
- ◇X_OUT_4
- ◇X_OUT_5
- ◇X_OUT_6
- ◇X_OUT_7
- ◇X_OUT_8
- ◇X_OUT_9
- ◇X_OUT_10
- ◇X_OUT_11
- ◇X_OUT_12
- ◇X_OUT_13
- ◇X_OUT_14
- ◇X_OUT_15

Y-AXIS HALF-SELECT DRIVERS (Y0 .. Y31)

32 Koinzidenz-Halbstromleitungen orthogonal zur X-Ebene.

- ◇Y_IN_0
- ◇Y_IN_1
- ◇Y_IN_2
- ◇Y_IN_3
- ◇Y_IN_4
- ◇Y_IN_5
- ◇Y_IN_6
- ◇Y_IN_7
- ◇Y_IN_8
- ◇Y_IN_9
- ◇Y_IN_10
- ◇Y_IN_11
- ◇Y_IN_12
- ◇Y_IN_13
- ◇Y_IN_14
- ◇Y_IN_15
- ◇Y_OUT_0
- ◇Y_OUT_1
- ◇Y_OUT_2
- ◇Y_OUT_3
- ◇Y_OUT_4
- ◇Y_OUT_5
- ◇Y_OUT_6
- ◇Y_OUT_7
- ◇Y_OUT_8
- ◇Y_OUT_9
- ◇Y_OUT_10
- ◇Y_OUT_11
- ◇Y_OUT_12
- ◇Y_OUT_13
- ◇Y_OUT_14
- ◇Y_OUT_15

DIAGONAL SENSE READ LOOP (45° S-PATTERN)

Differentielle mV-Leseschleife zur Erfassung des Ummagnetisierungsimpulses.

- ◇SENSE_POS
- ◇SENSE_NEG
- ◇SENSE_SHIELD
- ◇SENSE_GND
- ◇SENSE_TEST_TAP
- ◇SENSE_TERM_100R

INHIBIT WRITE LOOP & 4-CORNER BUS BARS

Z-Achsen Inhibit-Gegenstromleitung (Sperren von Schreibzugriffen) & Stützstäbe.

- ◇INHIBIT_IN
- ◇INHIBIT_RET
- ◇CORNER_STACK_NW
- ◇CORNER_STACK_NE
- ◇CORNER_STACK_SW
- ◇CORNER_STACK_SE

Standard: Acorn Risc PC Eurocard 3U (220x120 mm) • 40-Pin CLACK-BUS
Koinzidenzstrom-Speicherebene mit 45° Sense-Loop & Inhibit
Entwickler: Ing. Christian Buchhas & Dipl.-Ing. (FH) Peter Prikasky
Relay Computer Architecture Project

Sheet: /
File: core_plane_32x32.kicad_sch

Title: 16-Bit Core Memory Plane (32x32 = 1.024 Ferritkerne)

Size: A3	Date: 2026-11-01	**Rev: v1.5**
KiCad E.D.A. 9.0.8		Id: 1/1